Data Sheet September 25, 2007 FN6457.0

Dual Slot PCI-E Hot Plug Controllers

The ISL6113, ISL6114 both target the PCI-Express Add-in card hot swap application. Together with a pair of N-Channel and P-Channel MOSFETs, and two sense resistors per slot, either provides compliant hot plug power control to any combination of two PCI-Express X1, X4, X8 or X16 slots.

The ISL6113, ISL6114 feature a programmable current regulated (CR) maximum level for a programmable period to each voltage load so that both fault isolation protection and imperviousness to electrical transients are provided.

For each +12V supply, the CR level is set by a resistor value depending on the needs of the PCI-Express connector (X1, X4, X8 or X16) to be powered. This resistor is a sub-ohm standard value current sense resistor one for each slot and the voltage across this resistor is compared to a 50mV reference providing a nominal CR protection level adequately above the specific slot maximum limits. The 3.3V supply uses a 15mΩ sense resistor compared to a 50mV reference to provide 3.3A of maximum regulated current to all connector sizes. The 3.3VAUX is internally monitored and controlled to provide a nominal maximum of 1A of AUX output current.

The CR period for each slot is set by a separate external capacitor on the associated CFILTER pin. Once the CR period has expired, the IC then quickly turns off its associated FETs thus unloading the faulted card from the supply voltage rails. A nominal 3.3V must always be present on the AUXI pin for proper IC bias; this should be the 3.3VAUX supply if used, if not the AUXI pin is tied directly to the 3VMAIN supply. Both ICs employ a card presence detection input that disables the MAIN and AUX enabling inputs if it is not pulled low. Output voltage monitoring with both PCI-E Reset Not and Power Good Not reporting along with OC Fault reporting are provided. Whereas the ISL6113 has the same GATE drive and response characteristics as the ISL6112, the ISL6114 has a lower turn-on GATE drive current allowing for the use of smaller compensation capacitors and thus much faster response to Way Overcurrent (WOC) conditions. Additionally, the ISL6114 does not turn-on with the CR feature invoked as do the ISL6112, ISL6113 allowing for shorter CR programmed periods.The ISL6113, ISL6114 are footprint compatible for all common pins, but not entirely function compatible with the ISL6112's QFN package as there are I/O differences.

Features

- Dual PCI-E Slot Hot Swap Power Control and Distribution
- Highest Accuracy External R_{SENSE} Current Monitoring On Main Supplies
- Programmable Current Regulation Protection Function for X1, X4, X8, X16 Connectors
- Programmable Current Regulation Duration
- Programmable In-rush Protection During Turn-On
- Latch-off or Retry Modes After Failure
- Pb-free (RoHS Compliant)

Applications

- PCI-Express Servers
- Power Supply Distribution and Control
- Hot Swap/Electronic Breaker Circuits
- Network Hubs, Routers, Switches
- Hot Swap Bays, Cards and Modules

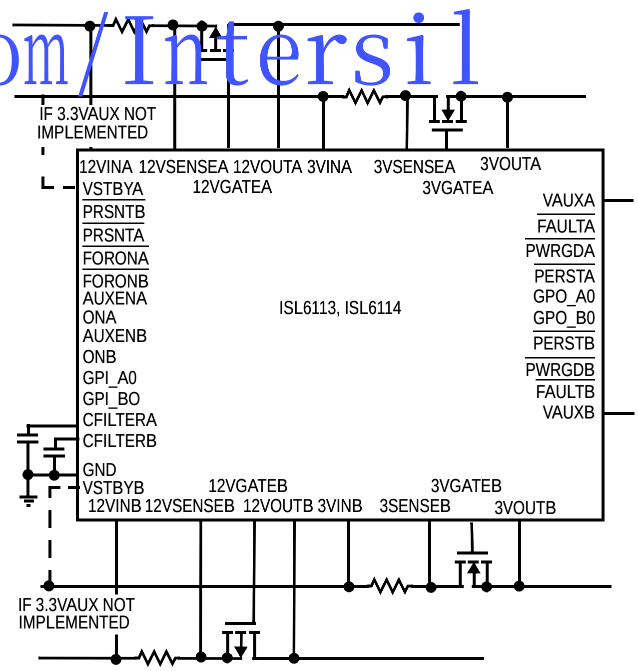


FIGURE 1. TYPICAL ISL6113, ISL6114 BLOCK DIAGRAM APPLICATION IMPLEMENTATION

Ordering Information

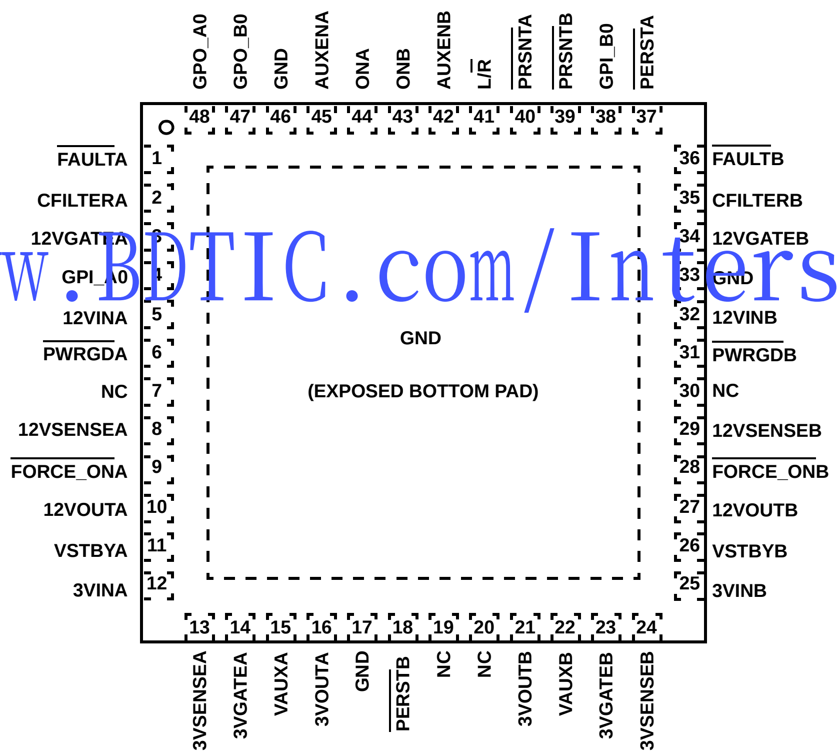
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6113IRZA	ISL6113 IRZ	-40 to +85	48 Ld 7x7 QFN	L48.7x7
ISL6113IRZA-T*	ISL6113 IRZ	-40 to +85	48 Ld 7x7 QFN Tape and Reel	L48.7x7
ISL6114IRZA	ISL6114 IRZ	-40 to +85	48 Ld 7x7 QFN	L48.7x7
ISL6114IRZA-T*	ISL6114 IRZ	-40 to +85	48 Ld 7x7 QFN Tape and Reel	L48.7x7
ISL6113EVAL1Z	ISL6113 Evaluation Platform			
ISL6114EVAL1Z	ISL6114 Evaluation Platform			

*Please refer to TB347 for details on reel specifications.

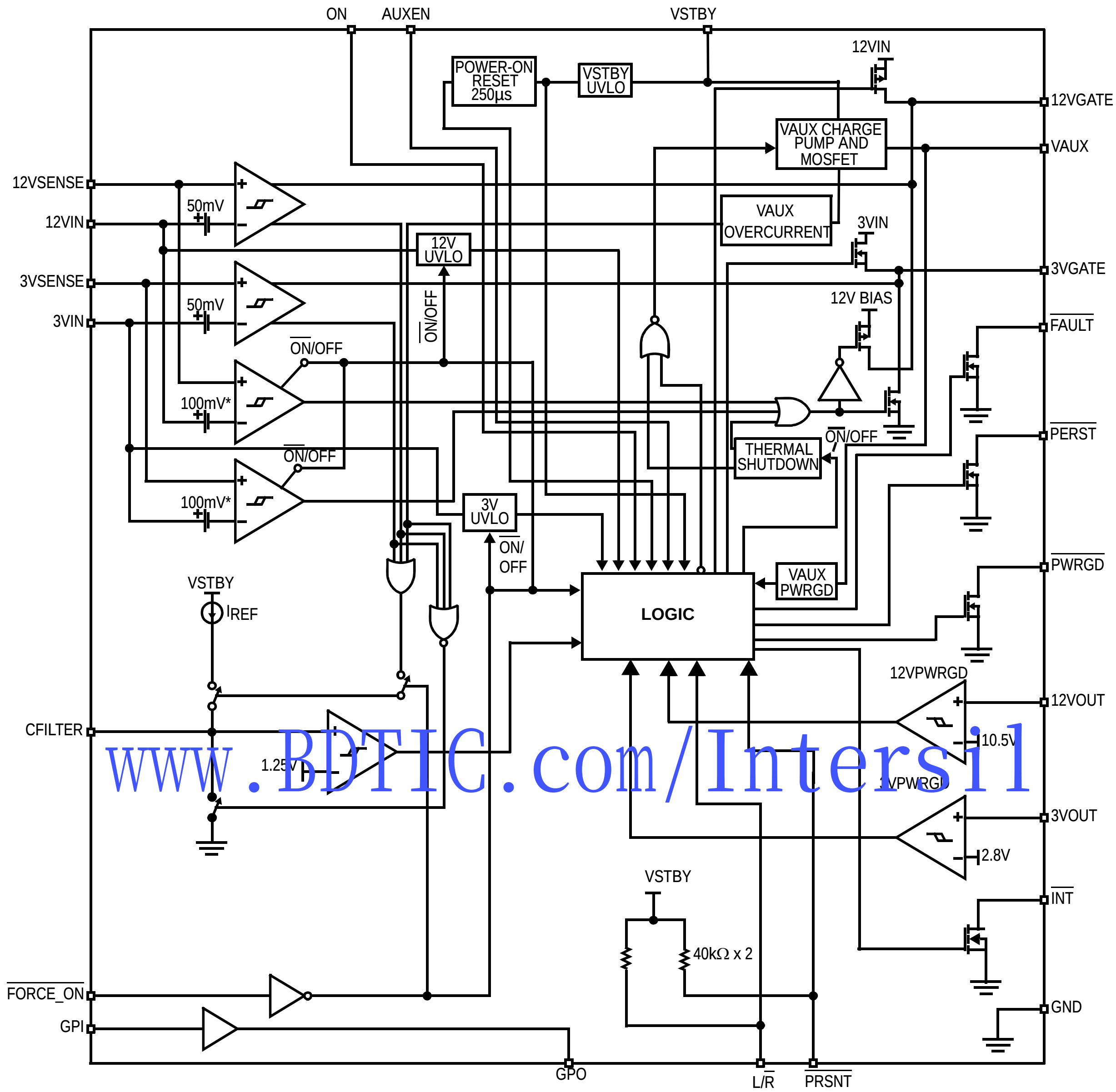
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL6113, ISL6114
(48 LD QFN)
TOP VIEW



Functional Block Diagram (1 Channel)



BOTH A AND B SLOTS SHARE THE L/R̄ PIN.

Pin Descriptions

PIN	NAME	FUNCTION
9, 28	FORCE_ONA, FORCE_ONB	Asserting a FORCE_ON input low will turn on the MAIN and AUX supplies to the respective slot in a forced mode over riding the ON input and the UV, OC and short circuit protections on those outputs. UVLO protection for the VSTBY input is not affected by the FORCE_ON pins. Asserting FORCE_ON will cause the PWRGD and FAULT outputs to enter their open-drain state. This input is internally pulled high to the VAUX rail. Functionality is disabled when PRSNT is high.
44, 43	ONA, ONB	Enable input for MAIN outputs use to enable or disable MAIN voltage supply (12V and 3.3V) outputs. Taking ONX low after a fault resets the respective slots Main Output Fault Latch. Functionality is disabled when PRSNT is high.
45, 42	AUXENA, AUXENB	3.3VAUX Enable Input, enables the respective VAUX output. Pulling AUXENX low after a fault resets the associated slot's VAUX fault latch. Functionality is disabled when PRSNT is high.
5, 32	12VINA,12VINB	Connect to 12VMAIN supply and high side of sense resistor. This is one of two pins for Kelvin connection to measure the 50mV CR Vth. An undervoltage lockout prevents the IC main supply function until 12VIN >10V. The current regulation threshold is set by connecting a sense resistor between this pin and 12VSENSE. When the current-limit threshold of IR = 50mV is reached, the 12VGATE pin is modulated to maintain a constant 50mV voltage across the sense resistor and thereby a constant current is passed into the load. If the 50mV threshold is maintained for CR duration, the circuit breaker is tripped and both GATE pins for the affected slot turn off the switch FETs and thus turn off the supplies to the slot.
8, 29	12VSENSEA, 12VSENSEB	12V current sense low side input. This is the second of two pins for Kelvin connection to the R_{SENSE} to measure the 50mV CR Vth. The CR limits are set by connecting a sense resistor between each of these pins and associated 12VIN pin.
10, 27	12VOUTA, 12VOUTB	12V output voltage monitor for UV condition. This is the voltage input downstream of the MOSFET that is delivered to the add-in card load.
12, 25	3VINA, 3VINB	Connect to 3VMAIN supply and high side of sense resistor. This provides one of two pins for Kelvin connection to measure the 50mV CR Vth. Undervoltage lockout (UVLO) prevents turn-on until 3VIN >2.75V. The current regulation threshold is set by connecting a sense resistor between this pin and 3VSENSE. When the current-limit threshold of IR = 50mV is reached, the 3VGATE pin is modulated to maintain a constant 50mV voltage across the sense resistor and thereby a constant current is passed into the load. If the 50mV threshold is maintained for the CR duration, the circuit breaker is tripped and both FETs for the affected slot are turned-off.
13, 24	3VSENSEA, 3VSENSEB	3.3V current sense low side input. This provides the second of two pins for Kelvin connection for measuring the 50mV CR Vth. The CR limits are set by connecting a sense resistor between each of these pins and associated 3VINX pin.
16, 21	3VOUTA, 3VOUTB	3.3V output voltage monitor for UV condition. This is the voltage downstream of the MOSFET that is delivered to the add-in card load.
1, 36	FAULTA, FAULTB	An open drain output which is pulled low whenever the CR duration has expired due to an OC fault condition on any of the MAIN or the AUX supplies or in the event of an IC over-temperature condition. If fault latch is invoked by a MAIN (+12V, +3.3V) supply fault, then it is reset by pulling the faulted slot's ON pin low. if fault was asserted because of an OC fault condition on the slot's AUX output then pulling the AUXEN input low will reset the latch. Both enabling inputs must be pulled low to clear a fault condition on both the MAIN and VAUX outputs of the same slot. Internal over-temperature limit is ~+140°C with a +20°C hysteresis.
15, 22	VAUXA, VAUXB	3.3VAUX output to the PCI-E slot: This output connects to the VAUX pin of the PCI-E connector through an internal 0.3Ω FET. This output is current regulated to ~1A.
11, 26	VSTBYA VSTBYB	3.3V bias input for the IC, and internal VAUX switches. V_{VSTBY} must always be present for proper IC bias, either from a dedicated 3.3V or 3VMAIN if AUX supply not implemented.
41	L/R	Latch-off or Retry bar input. Tying this input low invokes a periodic retry to turn-on after current regulation timer has expired on both slots. Leaving this pin open provides a latch-off operational mode after CR period has expired. In this mode turn-on is initiated by cycling the appropriate EN input(s). This pin is internally pulled up to VSTBY.
40, 39	PRSNTA, PRSNTB	The card presence detection input disables the operation of the FORCE_ON, ON and AUXEN inputs if not pulled to GND. If after turn-on, the PRSNT input goes high then all associated outputs (MAIN and AUX) are turned off immediately.
6, 31	PWRGDA, PWRGDB	A POWER GOOD NOT signal that is asserted low while all output voltages are compliant.
4, 38	GPI_A0, GPI_B0	~5ms debounced user attention input, driven by either a mechanical switch or digital signal form higher level controller.
48, 47	GPO_A0, GPO_B0	User attention output, that can be used to drive LEDs, alarms or other attention getting devices. Open drain with 90mA pull-down capability.

Pin Descriptions (Continued)

PIN	NAME	FUNCTION
3, 34	12VGATEA, 12VGATEB	12VMAIN gate drive output, connects to gate of an external P-Channel MOSFET. During power-up, this pin is pulled down with a 25µA (5µA for ISL6114) current to control the dv/dt ramp of the output voltage to the slot. During CR, the voltage on this pin is modulated to maintain a constant current into the load. During power-down or latch-off for an overcurrent fault, this pin is pulled high to 12VIN by internal sources.
14, 23	3VGATEA, 3VGATEB	3VMAIN gate drive outputs connects to gate of an external N-Channel MOSFET. During power-up this pin charges up with a 25µA (5µA for ISL6114) current to control the dv/dt ramp of the output voltage to the slot load. During CRTIM the voltage on this pin is modulated to maintain a constant current into the load. During power-down or latch-off for an overcurrent fault this pin is pulled low by internal sources.
37, 18	$\overline{\text{PERSTA}}$, $\overline{\text{PERSTB}}$	100ms delayed report of MAIN supplies output voltage compliance.
2, 35	CFILTERA, CFILTERB	A capacitor connected between each of these pins and ground sets the current regulated duration (tFILTER) for each slot. tFILTER is the amount of time for which a slot remains in current limit before its circuit breaker is tripped.
17, 33, 46	GND	IC ground reference
7,19, 20, 30	NC	No Connect

Absolute Maximum Ratings (Note 3)

12VIN, 12VSENSE, 12VOUT . . . . +14.5V
VSTBY, 3VIN, 3VSENSE, 3VOUT. . . . . +7V
12VGATE. . . . . -0.3V to 12VI
3VGATE. . . . . -0.3V to 12VI
Logic I/O . . . . -0.5V to +5.5V
VAUX Output Current . . . . .Short Circuit Protected
ESD Rating
Human Body Model 2kV
Machine Model. 200V
Charged Device Model 1kV

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld 7x7 QFN Package	27	3

Maximum Junction Temperature . . . .+150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

12VMAIN Supply Voltage Range. . . . . +12V ± 10%
3VMAIN Supply Voltage Range. . . . .+3.3V ± 10%
AUXI Supply Voltage Range . . . .+3.3V ± 10%
Temperature Range (T_A) . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
3. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

12VIN = 12V, 3VIN and VSTBY = +3.3V, $T_A = T_J$ = -40°C to +85°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MAIN CURRENT REGULATION						
Current Limit Threshold Voltages	VTHILIMIT	$V_{IN} - V_{SENSE}$	47.5	50	52.5	mV
Fast-Trip Threshold Voltages	VTHFAST	$V_{IN} - V_{SENSE}$ (ISL6113)	85	100	115	mV
		$V_{IN} - V_{SENSE}$ (ISL6114)	140	150	160	mV
VSENSE Input Current	ISENSE			0		µA
CFILTER Threshold Voltage	VFILTER		1.20	1.25	1.30	V
CFILTER Charging Current Nominal Current Limit Duration = C_{FILTER} x 550k	IFILTER	$V_{VIN} - V_{VSENSE} > V_{THILIMIT}$	2	2.5	3	µA
	tFILTER	CFILTER Open		10		µs
AUXILIARY CURRENT REGULATION						
Regulated Current Level	ILIM(AUX)	From end of ISC(TRAN) to CFILTER time-out	0.8	1	1.2	A
Output MOSFET Resistance VAUX MOSFET	$r_{DS(AUX)}$	I_{DS} = 375mA, T_J = +125°C			350	mΩ
Off-State Output Offset Voltage VAUX	VOFF(VAUX)	VAUX = Off, T_J = +125°C			40	mV
BIAS AND POWER GOOD						
Supply Current	ICC12	Enabled with no load current		0.9	1.5	mA
	ICC3.3	Enabled with no load current		0.1	0.2	mA
	ICCSTBY	Enabled with no load current		5	6	mA
12VIN, 3VIN, VSTBY Undervoltage Lockout Thresholds	VUVLO (12V)	12VIN increasing	8	9	10	V
	VUVLO (3V)	3VIN increasing	2.1	2.5	2.75	V
	VUVLO(STBY)	VSTBY increasing	2.8	2.9	2.96	V
Undervoltage Lockout Hysteresis 12VIN, 3VIN	VHYSUV			180		mV

Electrical Specifications 12VIN = 12V, 3VIN and VSTBY = +3.3V, $T_A = T_J$ = -40°C to +85°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Undervoltage Lockout Hysteresis VSTBY	VHYSSTBY			50		mV
Power-Good Undervoltage Thresholds	VUVTH(12V)	$12V_{OUT}$ decreasing	10.15	10.5	10.75	V
	VUVTH(3V)	$3V_{OUT}$ decreasing	2.7	2.8	2.9	V
	VUVTH(VAUX)	VAUX decreasing	2.55	2.8	3.0	V
Power-Good Detect Hysteresis	VHYSPG			30		mV
GATE DRIVE						
12VGATE Voltage	VGATE(12V)	Max Gate Voltage when Enabled	0		0.55	V
ISL6113 12VGATE Sink Current	IGATE (12VSINK)	Start Cycle	17	25	35	µA
ISL6114 12VGATE Sink Current		Start Cycle	3	5	7	µA
12VGATE Source Current (Fault Off) (Absolute Value)	IGATE (12VPULLUP)	Any fault condition (VDD – VGATE) = 2.5V	35	72		mA
3VGATE Voltage	VGATE(3V)	Min Gate voltage when Enabled	$12V_{IN}$ - 0.55		$12V_{IN}$	V
ISL6113 3VGATE Source Current	IGATE(3VCHARGE)	Start Cycle	17	25	35	µA
ISL6114 3VGATE Source Current		Start Cycle	3	5	7	µA
3VGATE Sink Current (Fault Off)	IGATE(3VSINK)	Any fault condition VGATE = 2.5V	80	105		mA
ANALOG I/O DC PARAMETERS						
GPO Pull-Down Current	I_{GPO_OUT}			80		mA
LOW-Level Input Voltage ON, AUXEN, GPI, FORCE_ON, PRSNT	VIL				0.8	V
Output LOW Voltage FAULT, PWRGD, GPO, PERST	VOL	IOL = 3mA			0.4	V
HIGH-Level Input Voltage ON, AUXEN, GPI,FORCE_ON, PRSNT	VIH		2.1		5	V
Internal Pull-ups to VSTBY (Note 4)	RPULLUP			40	50	kΩ
12VIN, 3VIN Input Leakage Current	ILKG,OFF XVIN	VSTBY = +3.3V, 12VIN = OFF; 3VIN = OFF		0.5	1	µA
Input/Output Leakage Current, ON, AUXEN, GPO, FORCE_ON, PERST,	IIL		-2		2	µA
Off-State Leakage Current FAULT, PWRGD, GPI	ILKG(OFF)	GPI I_{LKG} for these two pins measured with VAUX OFF	-2		2	µA
Output Discharge Resistance	RDIS (12V)	$12V_{OUT}$ = 6.0V		1400	1850	Ω
	RDIS (3V)	$3V_{OUT}$ = 1.65V		140	180	Ω
	RDIS (VAUX)	3VAUX = 1.65V		350	400	Ω
PERST Pull-Down Current when Asserted.	I_{PERST}	ONX is low		30		mA
THERMAL PROTECTION						
Over-temperature Shutdown and Reset Thresholds with Overcurrent on Slot	tOVER	T_J increasing, each slot		140		°C
		T_J decreasing, each slot		130		°C
Over-temperature Shutdown and Reset Thresholds, all other Conditions (all Outputs will Latch OFF)		T_J increasing, both slots		160		°C
		T_J decreasing, both slots		150		°C

Electrical Specifications

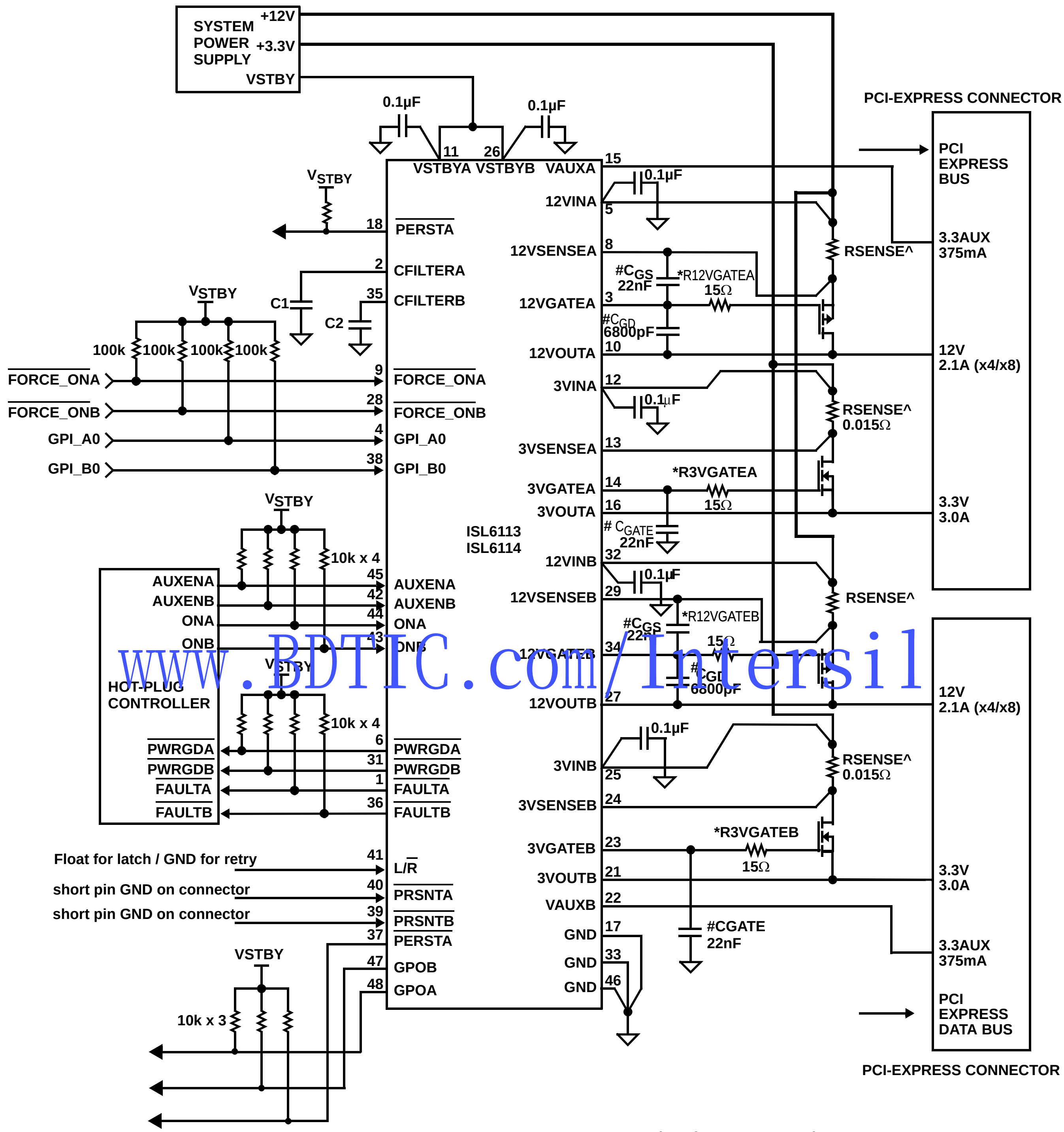
12VIN = 12V, 3VIN and VSTBY = +3.3V, $T_A = T_J$ = -40°C to +85°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/O TIMING PARAMETERS						
12V Current Limit Response Time	$t_{OFF(12V)}$	CGATE = 25pF VIN – VSENSE = 140mV		1	2.1	µs
3.3V Current Limit Response Time	$t_{OFF(3V)}$	CGATE = 25pF VIN – VSENSE = 140mV		0.3	1	µs
VAUX Current Limit Response Time	$t_{SC(TRAN)}$	VAUX = 0V, VSTBY = +3.3V		2.5		µs
Delay from MAIN Overcurrent to $\overline{\text{FAULT}}$ output	t_{PROP} (12V FAULT or 3V FAULT)	CFILTER = 0 VIN – VSENSE = 140mV		1		µs
Delay from VAUX Overcurrent to $\overline{\text{FAULT}}$ Output	t_{PROP}(VAUXFAULT)	$I_{LIM(AUX)}$ to $\overline{\text{FAULT}}$ output CFILTER = 0 VAUX output grounded		1		µs
ON, AUXEN, $\overline{\text{PRSNT}}$ Min Pulse Width	t_{min}			100		ns
Power-On Reset Time after VSTBY Becomes Valid	t_{POR}			250		µs
Auto-Retry Period	t_{RETRY}	R/L tied to GND, Any OC Event	0.75	1.4	3	s
Presence Detect Delay to Auto Enable	t_{PRSNT_ON}	$\overline{\text{PRSNT}}$ = high to low	4	6.5	9	ms
Presence Detect Delay to Disable	t_{PRSNT_OFF}	$\overline{\text{PRSNT}}$ = low to high		2.5		µs
GPI to GPO Propagation Delay	$t_{GPI-GPO}$	GPI high/low to GPO high/low	4	6	8	ms
Delay of Main Power Good to Reporting	t_{PVPERL}	$\overline{\text{PWRGD}}$ low to $\overline{\text{PERST}}$ high.	105	145	185	ms
Power Supply Disabled to PERST Low	t_{PERST}	ON Low to $\overline{\text{PERST}}$ Low		100		ns

NOTE:

4. Limits should be considered typical and are not production tested.

Typical Application Diagram



* Values for $R_{12VGATE}$ and R_{3VGATE} may vary depending upon the C_{GS} of the external MOSFETs.

\# These components are not required for ISL6113/4 operation but can be implemented for GATE output slew rate control (application specific)

- Bold lines indicate high current paths

^ R_{SENSE} value is application specific

ISL6113, ISL6114 Descriptions and Operational Explanation

These two ICs target the dual PCI-EXPRESS slot application for add-in cards in servers. Together with a pair of N and P-Channel MOSFETs, four high precision current sense resistors and a handful of passive components, the ISL6113, ISL6114 provide a PCI-E compliant hot plug control solution. These ICs use the Hot Plug Interface (HPI) for communicating, enabling, monitoring and reporting of UV conditions and OC and over temperature faults. Additionally they have a full complement of PCI-E specific I/O.

The ISL6113, ISL6114 share the same footprint as their sister part, the ISL6112, which features both SMI and HPI control and communication capabilities, neither of these two has serial bus capabilities. Whereas the ISL6113 has the same turn-on characteristics as the ISL6112, the ISL6114 uses a lower level of current sourcing on the GATE outputs (5µA vs the ISL6113's 25µA). This lower sourcing current allows the user to use less GATE capacitance for in-rush current and GATE ramp control than the ISL6113 to achieve similar turn-on characteristics. This reduced capacitance in turn provides for a faster turn-off of the MAIN supplies by the ISL6114 in the event of an OC fault than is possible with the ISL6113.

Bias, Power-On Reset and Power Cycling

The ISL6113, ISL6114 utilizes the VSTBY pins as the only IC bias supply source. For systems without a dedicated 3.3V auxiliary supply, the 3VMAIN supply is to be used for the IC bias. A Power-On Reset (POR) cycle is initiated after VSTBY rises above its UVLO threshold and remains satisfied for t_{POR}, ~250µs. If VSTBY is recycled, the ISL6113, ISL6114 enters a new power-on-reset cycle. VSTBY must be the first supply voltage applied followed by the MAIN supply inputs. During t_{POR}, all outputs remain off. PCI-Express (PCI-E) compliance requires that the connector power must be off prior to and during insertion and during removal of a PCI-E board. Before the add-in board is properly inserted into or removed from a connector, the FET switches are turned off via the enabling inputs (ON_X and AUXEN_X). In the event of an improper insertion or removal and to ensure that the power is off when necessary, the ISL6113, ISL6114 has a present input ($\overline{PRSNT}$) per slot that overrides and disables the enabling inputs if $\overline{PRSNT}$ is not pulled low by having a card fully inserted into the slot to complete the pull-down circuit. The $\overline{PRSNT}$ pin must be a last to make, first to break connection to ensure compliance.

Enabling the VAUX Outputs

Upon asserting an AUXEN input, the related output turns-on the internal power switch between the VSTBY supply and its load. The turn-on is slew rate limited and invokes the ICs current regulation feature so as to not droop the supply due to in-rush current loading. Figure 2 illustrates the ISL6113 AUX turn-on performance into a 100Ω, 150µF load with the in-rush load current being limited to ~1A.

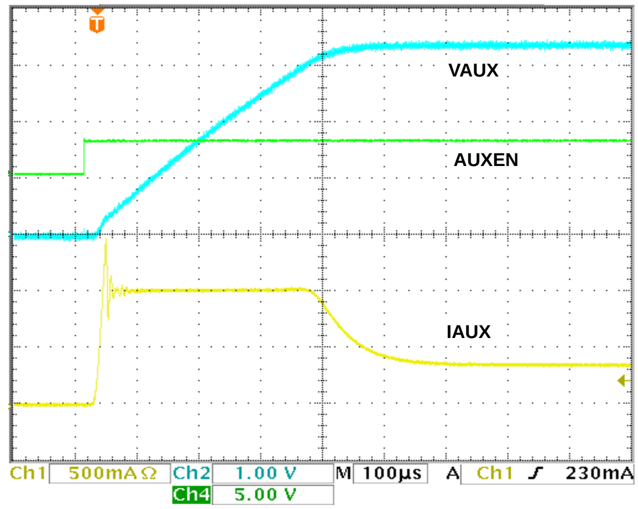


FIGURE 2. VAUX TURN-ON R_{LOAD} = 10Ω, C_{LOAD} = 100µF

Standby Mode

Standby mode is entered when one or more of the MAIN supply inputs ($12V_{IN}$ and/or $3V_{IN}$) is absent, below its respective UVLO threshold or OFF. The ISL6113, ISL6114 also has 3.3V auxiliary outputs (VAUX), satisfying an optional PCI Express requirement. These outputs are fed from the VSTBY input pins and controlled by the AUXEN input pins and are independent of the MAIN outputs. Should IC be in standby mode the VAUX switch will function as long as V_{VSTBY} is compliant. Prior to standby mode, ONA and ONB inputs must be deasserted or else the ISL6113, ISL6114 will assert its $\overline{FAULT}$ outputs.

Enabling the MAIN GATE Outputs

The related AUXEN must be active for the MAIN supplies to be enabled otherwise they will be latched off. When a slots MAIN supplies are off, the 12VGATE pin is held high with an internal pull-up to the 12VIN voltage. Similarly, the 3VGATE pin is internally held low to GND. With an add-in card properly in place, when an ON_X pin is signaled high, the ISL6113, ISL6114 enables control of one slot turning on one pair of FETs via the 3VGATE and 12VGATE pins. The FET gates are charged with a ∓25µA (∓5µA for the ISL6114) current sink/source pulling the 12VGATE pin to ground and the 3VGATE pin is charged to ~12VIN thereby enhancing both of the MAIN supply FET switches.

Estimating In-Rush Current and V_{OUT} Slew Rate at Start-Up

The expected in-rush current can be estimated by using Equation 1:

$$\text{ISL6113 - } I_{INRUSH}\text{Nominally} = 25\mu A\left(\frac{C_{LOAD}}{C_{GATE}}\right)$$

$$\text{ISL6114 - } I_{INRUSH}\text{Nominally} = 5\mu A\left(\frac{C_{LOAD}}{C_{GATE}}\right) \quad \text{(EQ. 1)}$$

With 25µA and 5µA being the GATE pin charge current for

the ISL6113, ISL6114 respectively, C_{LOAD} is the load capacitance, and C_{GATE} is the total GATE capacitance including C_{ISS} of the external MOSFET and any external capacitance connected from the GATE output pin to the GATE reference, GND or source.

An estimate for the output slew rate of 3.3V outputs and 12V outputs where there is little or no external 12VGATE output capacitors, can be taken from Equation 2:

$$VOUTdv/dt = \frac{I_{LIM}}{C_{LOAD}} \quad \text{(EQ. 2)}$$

where I_{LIM} = 50mV/R_{SENSE} and C_{LOAD} is the load capacitance. Note: As a consequence, the CR duration, t_{FILTER} must be programmed to exceed the time it takes to fully charge the output load to the input rail voltage level.

MAIN Outputs (Start-up Delay and Slew-Rate Control)

The 3.3V outputs act as source followers. In this mode of operation, $V_{SOURCE} = [V_{GATE} - V_{TH(ON)}]$ until the associated output reaches 3.3V. The voltage on the gate of the MOSFET will then continue to rise until it reaches 12V, which ensures minimum $r_{DS(ON)}$. For the 12V outputs, when the MOSFET is optionally configured as a Miller integrator to adjust the V_{OUT} ramp time by having a C_{GD}, which is connected between the MOSFET's gate and drain. In this configuration, the feedback action from drain to gate of the MOSFET causes the voltage at the drain of the MOSFET to slew in a linear fashion at a rate estimated by Equation 3:

$$\text{ISL6113 } VOUTdv/dt = \frac{25\mu A}{C_{GD}}$$

$$\text{ISL6114 } VOUTdv/dt = \frac{5\mu A}{C_{GD}} \quad \text{(EQ. 3)}$$

Tables 1 and 2 approximate the output slew-rate for various values of C_{GATE} when start-up is dominated by GATE capacitance (external C_{GATE} from GATE pin to ground plus C_{GS} of the external MOSFET for the 3.3V rail; C_{GD} for the 12V rail).

TABLE 1. ISL6113 3.3V AND 12V OUTPUT SLEW-RATE SELECTION FOR GATE CAPACITANCE DOMINATED START-UP

| IGATE | = 25µA	
CGATE or C_{GD}	**dv/dt (LOAD)**
0.01µF*	2.5V/ms
0.022µF*	1.136V/ms
0.047µF	0.532 V/ms
0.1µF	0.250V/ms

*Values in this range will be affected by the internal parasitic capacitances of the MOSFETs used and should be verified empirically.

TABLE 2. ISL6114 3.3V AND 12V OUTPUT SLEW-RATE SELECTION FOR GATE CAPACITANCE DOMINATED START-UP

| IGATE | = 5µA	
CGATE or C_{GD}	**dv/dt (LOAD)**
0.01µF*	0.5V/ms
0.022µF*	0.23V/ms
0.047µF	0.106 V/ms
0.1µF	0.050V/ms

*Values in this range will be affected by the internal parasitic capacitances of the MOSFETs used and should be verified empirically.

During turn-on, the ISL6113 invokes the current regulation (CR) feature to limit inrush current whereas the ISL6114 disables the CR feature during turn-on thus allowing a shorter programmed t_{FILTER}. Both ICs monitor for a severe or Way Overcurrent (WOC) condition such as a short at this time.

Note that all of these performance estimates and guidelines are useful only for first order time and loading expectations, as they do not look at other significant loading factors. Figures 3 through 11 realistically illustrate the discussed turn-on performance topic with the noted loading and compensation conditions. Notice the degree of control over the in-rush current and the GATE ramp rate as the C_{GD} and C_{GS} values are changed providing for highly customized turn on characteristics.

In some scope shots although the C_{FILTER} shows a ramping in the absence of excessive displayed loading current the C_{FILTER} is responding to the other MAIN supply current that is not displayed.

All scope shots were taken from the ISL6113EVAL1Z or ISL6114EVAL1Z platform with any component changes are noted.

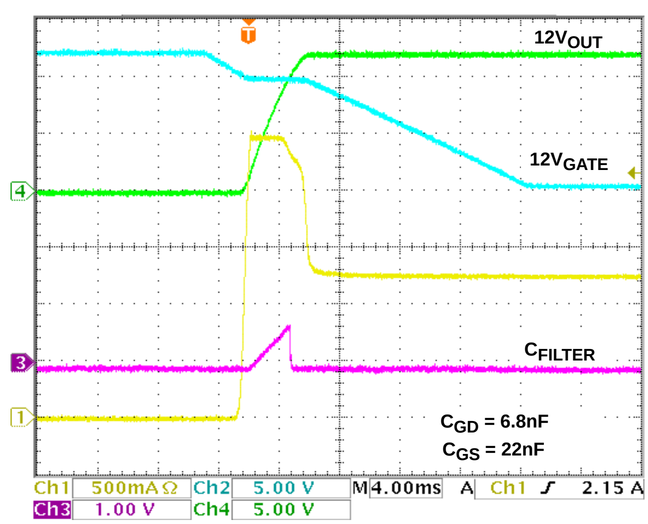


FIGURE 3. ISL6113 12VMAIN START-UP R_{LOAD} = 10Ω, C_{LOAD} = 470µF

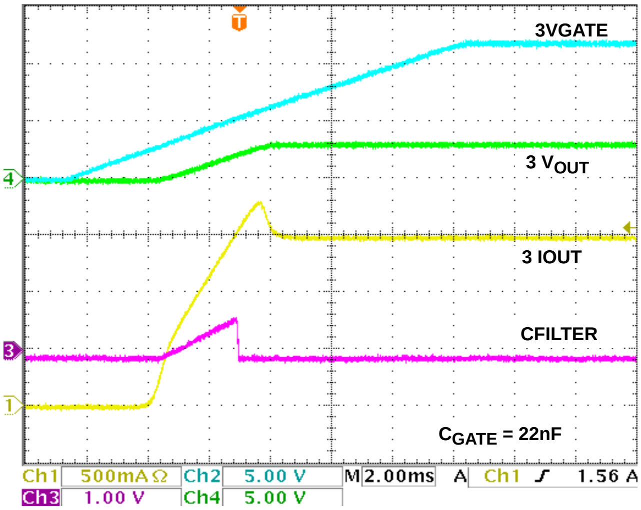


FIGURE 4. ISL6113 3VMAIN START-UP $R_{LOAD} = 2\Omega$, $C_{LOAD} = 470\mu F$

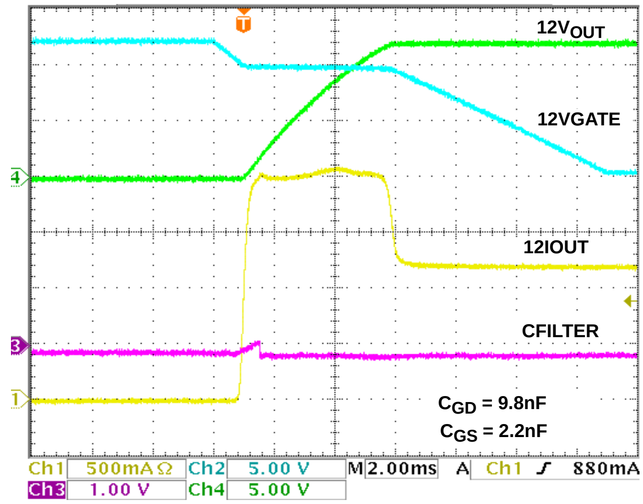


FIGURE 7. ISL6113 12VMAIN START-UP $R_{LOAD} = 10\Omega$, $C_{LOAD} = 470\mu F$

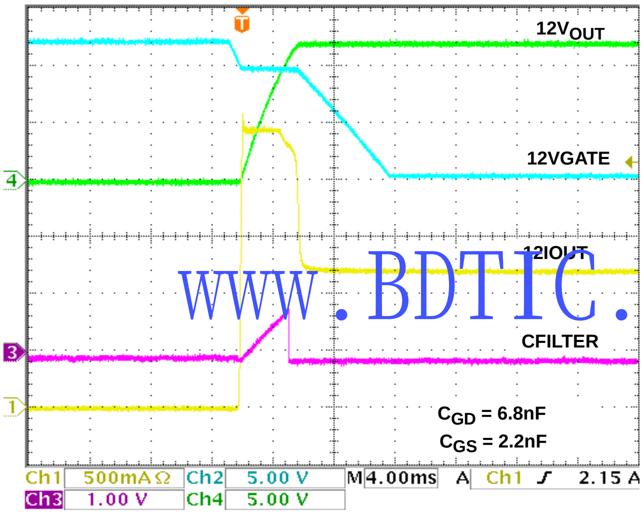


FIGURE 5. ISL6113 12VMAIN START-UP $R_{LOAD} = 10\Omega$, $C_{LOAD} = 470\mu F$

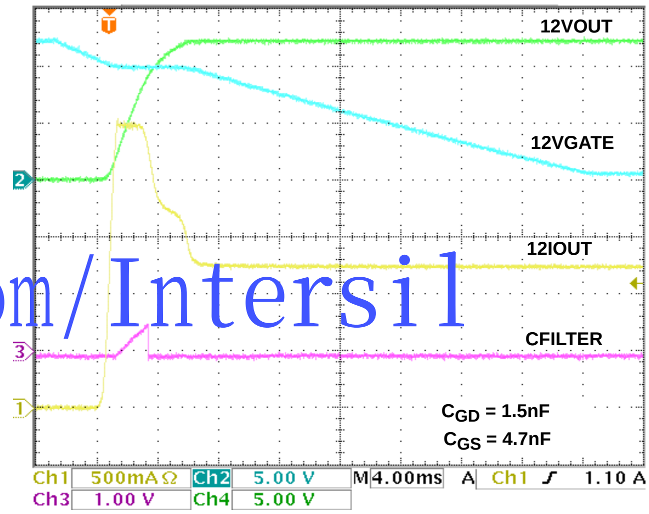


FIGURE 8. ISL6114 12VMAIN START-UP $R_{LOAD} = 10\Omega$, $C_{LOAD} = 470\mu F$

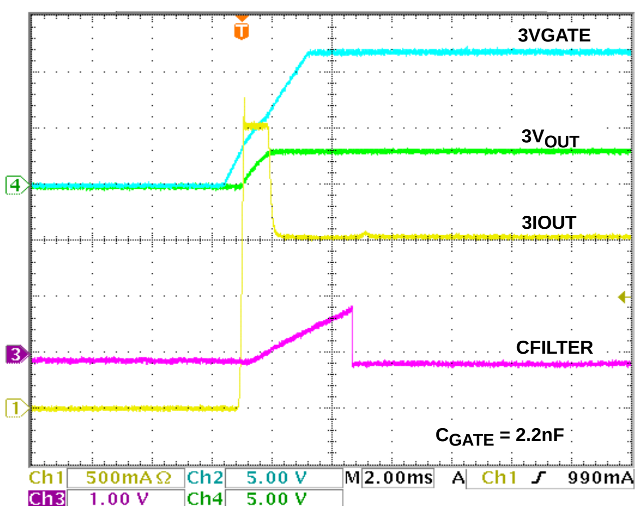


FIGURE 6. ISL6113 3VMAIN START-UP $R_{LOAD} = 2\Omega$, $C_{LOAD} = 470\mu F$

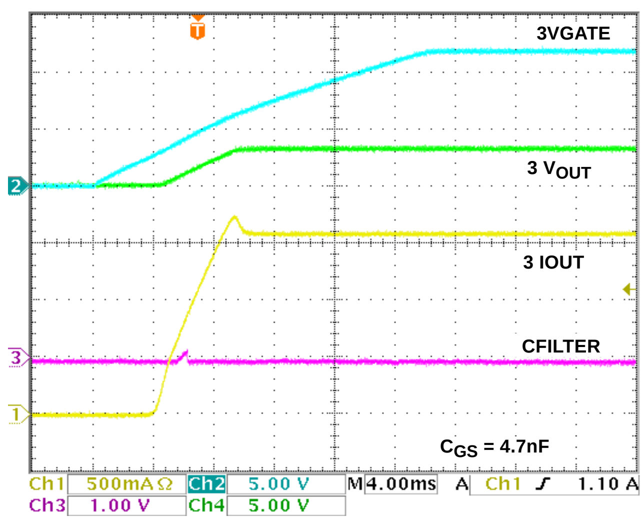


FIGURE 9. ISL6114 3VMAIN START-UP $R_{LOAD} = 2\Omega$, $C_{LOAD} = 470\mu F$

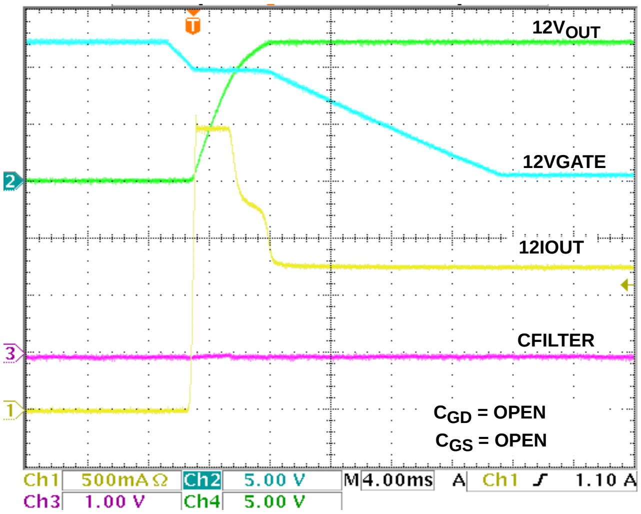


FIGURE 10. ISL6114 12VMAIN START-UP R_{LOAD} = 10Ω, C_{LOAD} = 470µF

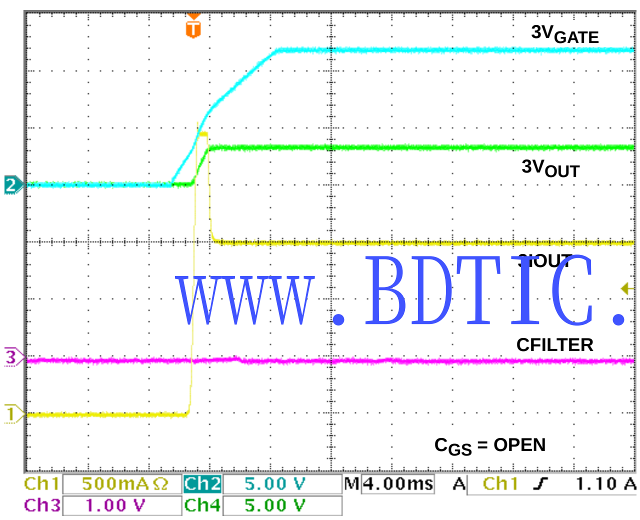


FIGURE 11. ISL6114 3VMAIN START-UP R_{LOAD} = 2Ω, C_{LOAD} = 470µF

Current Regulation (CR) Function

The ISL6113, ISL6114 provides a current limiting function that protects the input voltage supplies against excessive current loads, including short circuits during turn-on (MAIN supplies shown in previous Figures 3 through 11) and during static operation for both MAIN (Figures 12 through 15) and AUX supplies (Figures 16 and 17). When during static operation, any load current causes >$V_{THILIMIT}$ (nominally 50mV) drop across a sense resistor thus exceeding the programmed CR limit, the ISL6113, ISL6114 enters its CR mode where it regulates the load current to the programmed level by modulating the gate of the related FET switch into the linear region of operation to maintain 50mV across the sense resistor for the programmed t_{FILTER} duration. However, should the load current cause a V_{RSENSE} > V_{THFAST}, the outputs are immediately shut off with no t_{FILTER} delay, as shown in Figures 14 and 15. If the ISL6113, ISL6114 latches off due to the t_{FILTER} expiring, then the FETs are turned-off more aggressively than if signaled from the linear region with approximately 80mA of GATE current to ensure faster isolation from the voltage bus. This is also true when turning off from a WOC event.

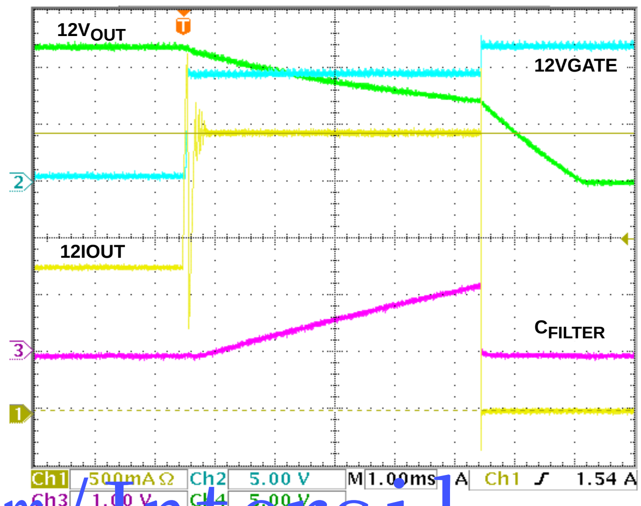


FIGURE 12. ISL6113 12VMAIN CR AND SHUTDOWN

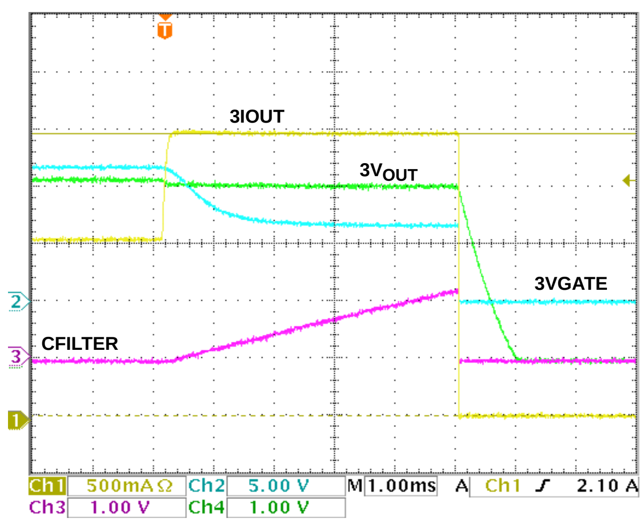


FIGURE 13. ISL6113 3VMAIN CR AND SHUTDOWN

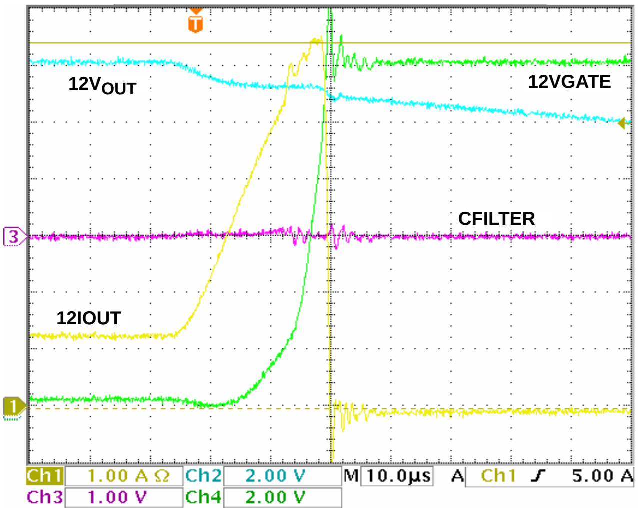


FIGURE 14. ISL6113 12VMAIN WOC SHUTDOWN

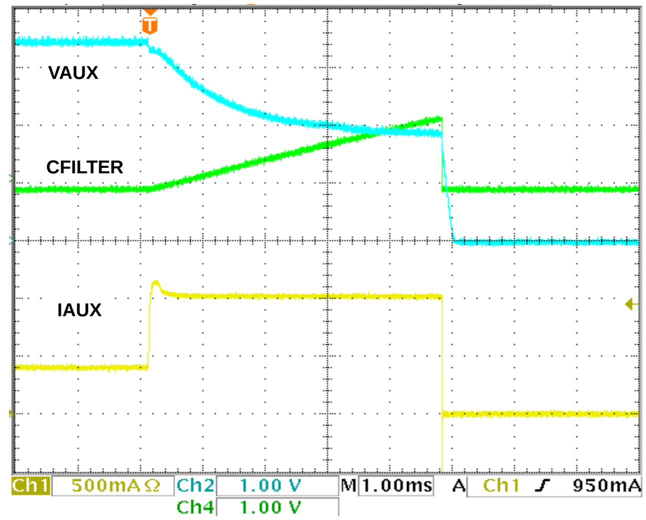


FIGURE 16. VAUX OC REGULATION AND SHUTDOWN

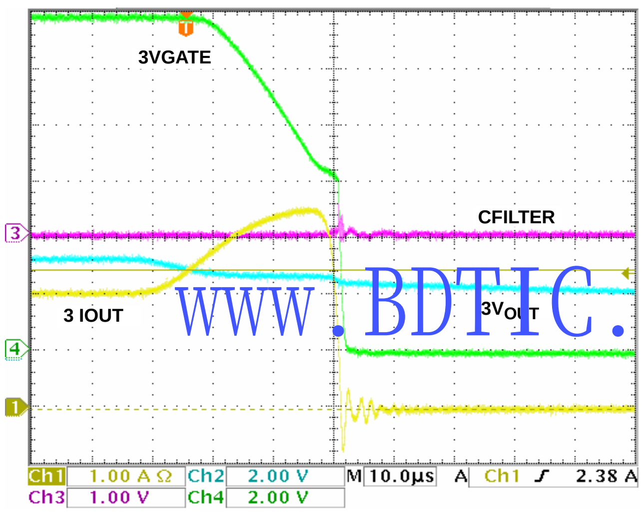


FIGURE 15. ISL6113 3VMAIN WOC SHUTDOWN

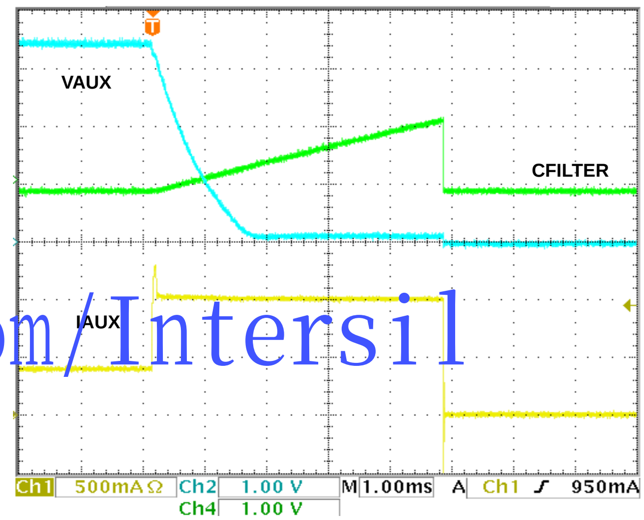


FIGURE 17. VAUX WOC REGULATION AND SHUTDOWN

The VAUX outputs have a different circuit-breaker function. The VAUX circuit breakers do not incorporate a fast-trip detector, instead they regulate the current into a fault to avoid exceeding their operating current limit. The circuit breaker will trip due to an overcurrent on VAUX when the programmable CR duration timer, t_{FLT} expires. This use of the t_{FLT} timer prevents the circuit breaker from tripping prematurely due to brief current transients. See Figures 16 and 17 for illustrations of the VAUX protection performance into an over current (OC) and more severe OC condition respectively. The ISL6113, ISL6114 AUX current control responds proportionally to the severity of the OC condition resulting in appropriately fast VAUX pull down and current regulation until t_{FILTER} has expired.

In the fault latch mode set by leaving L/$\overline{R}$ pin open, following a fault condition, the outputs can be turned on again via the ON inputs (if the fault occurred on one of the MAIN outputs), via the AUXEN inputs (if the fault occurred on the AUX outputs), or by cycling both ON and AUXEN (if faults occurred on both the MAIN and AUX outputs). When the circuit breaker trips, $\overline{FAULT}$ will be asserted. In the fault retry mode, set by grounding the L/$\overline{R}$ pin the ISL6113, ISL6114 will initiate an automatic restart about every 1.5s until successful.

The ISL6113, ISL6114 current regulation duration (t_{FILTER}) is set by external capacitors at the CFILTER pins to GND. Once the CR mode is entered, the external cap is charged with a 2.5µA current source to 1.25V. Once this threshold has been reached the IC then turns-off all fault the related FETs and sets the $\overline{FAULT}$ output low. For a desired t_{FILTER}, the value for $C_{CFILTER}$ is given by Equation 4:

$$C_{FILTER} = \frac{\text{nominal } t_{FILTER}}{500k\Omega} \quad \text{(EQ. 4)}$$

where 500kΩ is (nominal V_{FILTER}/nominal I_{FILTER}) and where t_{FILTER} is the desired response time with the values for I_{FILTER} and V_{FILTER} being found in the ISL6113, ISL6114's "Electrical Specifications Table" on page 6. See Table 3 for nominal t_{FILTER} times for given C_{FILTER} cap values.

For the ISL6113, there is a minimum t_{FILTER} consideration since the ISL6113 has its CR feature invoked as it turns-on the FETs into the load. There is a maximum bulk capacitance specified for each power level supported that needs to be charged at the CR limit. This in-rush current time must be considered when programming the t_{FILTER}.

TABLE 3.

NOMINAL t_{FILTER} DURATION	
C_{FILTER} CAPACITANCE (µF)	TIME (ms)
Open	0.01
0.01	5
0.022	11
0.047	24
0.1	50

NOTE: Nom. CR_DUR = C_{FILTER} cap (µF) * 500kΩ.

Holding the CFILTER pin low will increase the CR duration indefinitely. This feature may be useful in trouble shooting, or evaluation. If this is invoked be cautious not to violate the SOA of the pass FETs.

Power-Down Cycle

When signaled off, the GATE pins are discharged/charged with a 25µA for ISL6113 (5µA for ISL6114) current sink/source to ramp down the supplies in a controlled fashion. When a slot is turned off, internal switches are connected to the outputs $12V_{OUT}$ and $3V_{OUT}$ providing a discharge path for load capacitance. This ensures that the outputs are pulled to GND, thereby ensuring 0V on slot connectors during removal or insertion of add-in cards.

Thermal Shutdown

The internal VAUX switches are protected against damage not only by current limiting, but by a dual mode over-temperature protection scheme as well. Each slot controller on the ISL6113, ISL6114 is thermally isolated from the other. Should an overcurrent condition raise the junction temperature of one slots controller and pass switch > T_{OVER} (nominally +140°C), all of the outputs for that slot will be shut off and the slots FAULT output will be asserted. The other slots operating condition will remain unaffected. However, should the ISL6113, ISL6114's die temperature exceed +160°C, all outputs for both slots will be shut off, whether or not a current limit condition exists.

Special I/O

Power Good Outputs (PWRGD)

The ISL6113, ISL6114 have two open-drain, active-low PWRGD outputs that must be pulled up to VSTBY. This output will be asserted when a slot has been enabled and the 12VMAIN, 3VMAIN and VAUX outputs exceed their respective V_{UVTH} levels.

PCI-E Reset Outputs (PERST)

A PCI-Express specific output, the ISL6113, ISL6114 have two open-drain, active-low PERST outputs that must be pulled up to VSTBY. Upon enabling, the assertion high of PERST is delayed a minimum of 100ms (t_{PVPERL}) from the power rails achieving minimum specified operating limits for stability of supplies and REFCLK. Once high the card functions can safely start-up. PERST is immediately pulled low when the power supply is disabled.

Force_On Inputs (FORCE_ON)

These inputs are provided to facilitate system diagnostics or evaluation when using the ISL6113, ISL6114. Asserting a FORCE_ON input will turn on all three of the slots outputs, while over riding all three supplies overcurrent, the MAIN supplies UV protections, on-chip thermal protection for the VAUX supplies and disable the PWRGD and FAULT outputs. Asserting the FORCE_ON inputs will not disable the $V_{UVLO(STBY)}$. If not used, each pin should be connected to VSTBY.

General Purpose I/O (GPI, GPO)

Two pairs of pins on the ISL6113, ISL6114 are available for buffered driving. Both of these are compliant to 3.3V. If unused, connect each GPI pin to GND. The GPI pins are 5ms debounced for filtering and the GPO are open drain capable of 90mA pull down current for attention getting devices in accordance with the PCI-Express specifications.

Latch/Retry Operation Toggle (L/R)

This input pin is tied to GND for a ~1.5s retry period after fault. If left open or tied high to VSTBY, the ISL6113, ISL6114 will latch off upon a fault.

Board Present Input (PRSNT)

The PRSNT input is used to detect the presence of an add-in card in the slot. In systems where Manual Retention Latch (MRL) is not implemented, this input detects when an add-in card is properly inserted into the slot via the last make, staggered length PRSNT connection on the add-in card connector. This input must be pulled to ground through the add-in card ensuring all connections have been made between the connector and the card in order to enable 3.3VAUX turn-on. This pin function can be defaulted by tying to GND. PRSNT not being pulled low overrides and disables all FORCE_ON, ON and AUXEN commands and for ~5ms after being pulled low. In systems where MRL is implemented this input is connected to the MRL sensor. The MRL Sensor allows monitoring of the position of the MRL and therefore allows detection of unexpected openings of the MRL. These inputs are internally pulled up to the VSTBY rail. All I/O are valid at VSTBY <1V.

PCI-Express Application Recommendations

For each of the 3VMAIN and +12VMAIN supply, the CR level is set by an external sense resistor value depending on the maximum specified power for the various sizes of the PCI-Express connector and application implemented (X1, 10W or 25W; X4, X8, 25W; X16, 25W or 75W; and X16 Graphic-ATX, 150W). The power rating is a combination of both main and the optional auxiliary supplies. This sense resistor is a low sub-1Ω standard value current sense resistor (one for each slot) and the voltage across this resistor is compared to a 50mV reference. On the 12VMAIN, for a10W connector, a 75mΩ sense resistor provides a nominal CR level of 0.66A, 32% above the 0.5A maximum specification; for a 25W connector, a 20mΩ sense resistor provides a nominal CR level of 2.5A, 19% above the 2.1A maximum specification; for a 75W connector a 8mΩ sense resistor provides a nominal CR level of 6.25A, 14% above the 5.5A maximum specification; for a X16 Graphics-ATX 150W card, a 7mΩ sense resistor provides a nominal CR level of 7.1A, 14% above the 6.25A maximum specification. The 150W is provided by 2 slots, each providing up to a maximum of 75W from the 12VMAIN as this specialized type of card does not consume 3VMAIN or AUX supply power. The 3.3V supply uses a 15mΩ sense resistor compared to a 50mV reference to provide a nominal CR of 3.3A or 11% above the 3A maximum specification load across all sizes and power levels of the connector.

Table 4 provides recommended 12VMAIN sense resistor values for particular power levels.

TABLE 4.

NOMINAL CURRENT REGULATION LEVEL		
12VMAIN R_{SENSE} (mΩ)	12VMAIN CR (A)	PCI-E ADD IN BOARD POWER LEVEL SUPPORTED (W)
75	0.7	10
20	2.5	25
8	6.2	75
7	7	150

NOTE: CR Level = VTH_{ILIMIT}/R_{SENSE}.

Providing a nominal CR protection level above the maximum specified limits of the card ensures that the card is able to draw its maximum specified loads, and, in addition, have enough headroom before a regulated current limiter is invoked to protect against transients and other events. This headroom margin can be adjusted up or down by utilizing differing values of sense resistor.

Using the ISL6113EVAL1Z, ISL6114EVAL1Z Platform

Description and Introduction

The primary ISL6113, ISL6114 evaluation platform is shown in Figures 37 and 38 both photographically and schematically. This evaluation board highlights a PCB layout that confines all necessary active and passive components in an area 12mmx55mm. This width is smaller than the specified PCI-Express socket to socket spacing allowing for intimate co-location of the load power control and the load itself.

Around the central highlighted layout are numerous labeled test points and configuration jumpers. Where there are node names such as, AO(L/$\overline{R}$) the pin name in parentheses relates to the ISL6113, ISL6114. The ISL6113, ISL6114 share an evaluation platform with the ISL6112 as all three parts have a common pinout for the common pin functions. The specific evaluation board as ordered and received will reflect the part number in the area below the Intersil logo either by label or silk screened lettering. For those pins not common across the ISL6112 and ISL6113, ISL6114 in the bottom left corner there is a matrix detailing the differences.

After correctly biasing the evaluation platform as noted through the 6 banana jacks, turning on VSTBY first then the other MAIN supplies in any order. With the appropriate signaling to the AUXEN and ON inputs the user should see turn-on waveforms as shown previously. The addition of external current loading is necessary to demonstrate the OC and WOC response performance.

Figures 18 and 19 demonstrate some of the PCI-E specific and additional I/O functionality. Figure 18 shows the PRSNT pin being signaled low then the $12V_{OUT}$ and $3V_{OUT}$ outputs turning on automatically as the ON input is already asserted. Power good is signaled once the $12V_{OUT}$ and $3V_{OUT}$ meet their respective VUVVth levels. After the time period t_{PVPERL} the PCI-E specific reset signal output, PERST is asserted. Figure 19 shows the GPI to GPO ~6ms functionality. Figure 20 shows the retry period operation. Approximately every 1.5s the IC attempts to restart into a faulty load until finally being able to turn-on fully into a normal load. This retry mode is invoked with $\overline{R}$/L input tied low.

ISL6113EVAL1Z, ISL6114EVAL1Z Errata

GPO_A0 and GPO_BO labeling is reversed. Correct labeling shown on evaluation board photograph in Figure 37.

Caution: The ISL6113EVAL1Z, ISL6114EVAL1Z gets very hot to the touch after operating it for a few minutes. Hottest areas marked on evaluation board.

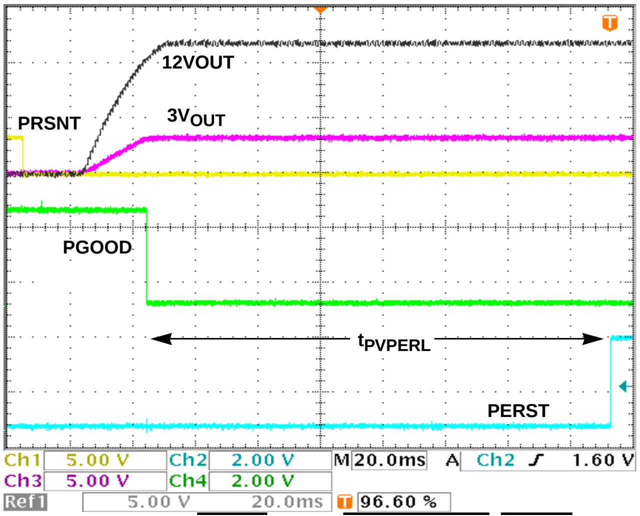


FIGURE 18. $\overline{\text{PRSNT}}$, V_{OUT}, $\overline{\text{POWERGOOD}}$, $\overline{\text{PERST}}$

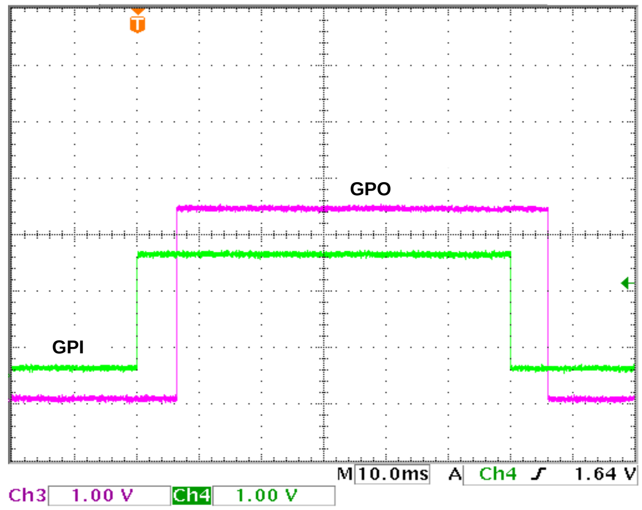


FIGURE 19. GPI TO GPO FUNCTIONALITY

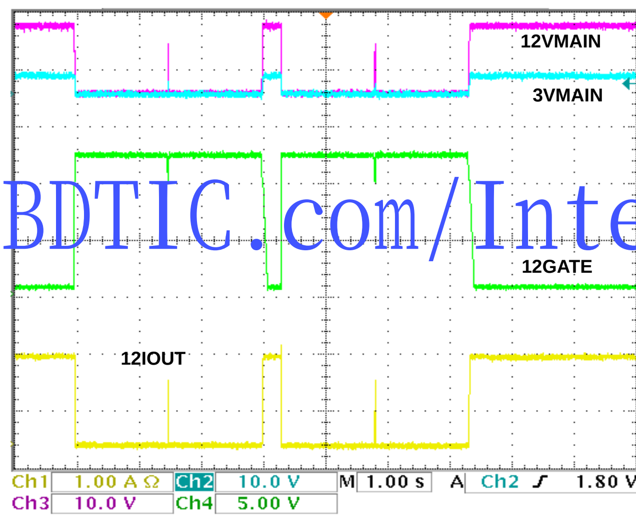


FIGURE 20. RETRY MODE OPERATION

Typical Performance Curves

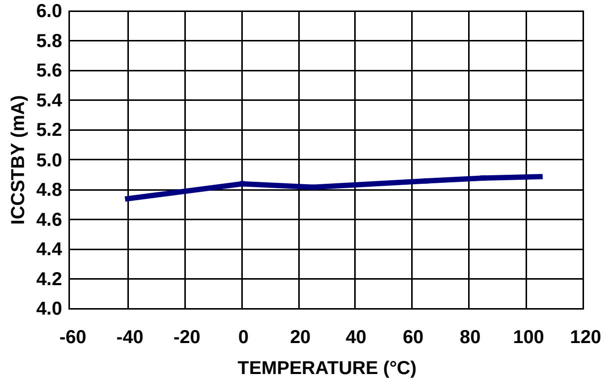


FIGURE 21. ICCSTBY CURRENT vs TEMPERATURE

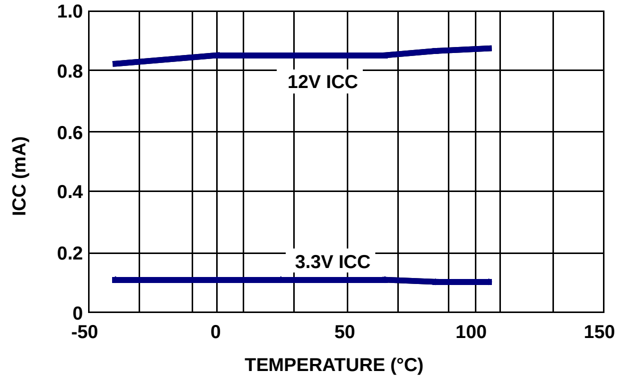


FIGURE 22. ICC CURRENT vs TEMPERATURE

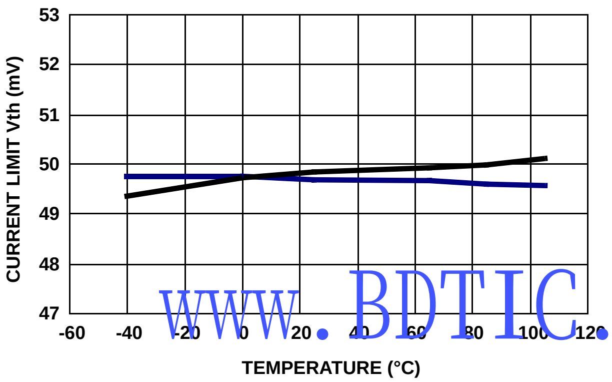


FIGURE 23. CURRENT LIMIT THRESHOLD VOLTAGE vs TEMPERATURE

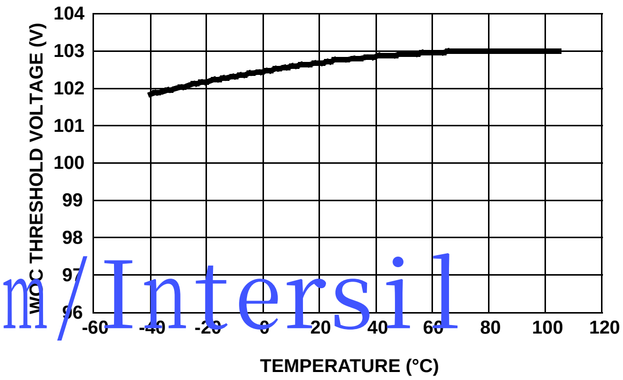


FIGURE 24. FAST TRIP THRESHOLD VOLTAGE vs TEMPERATURE

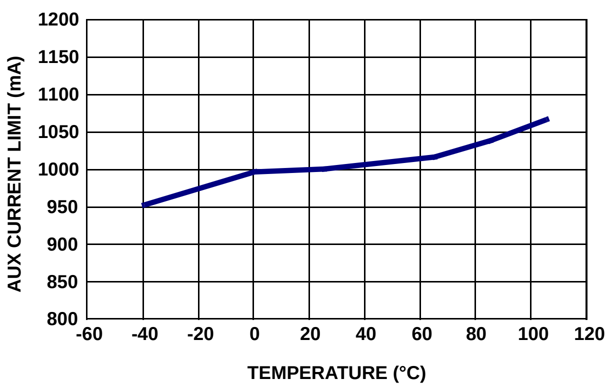


FIGURE 25. AUX CURRENT LIMIT vs TEMPERATURE

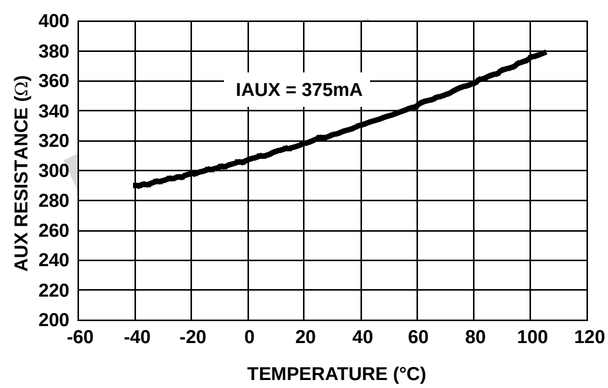


FIGURE 26. AUX $r_{DS(ON)}$ vs TEMPERATURE

Typical Performance Curves (Continued)

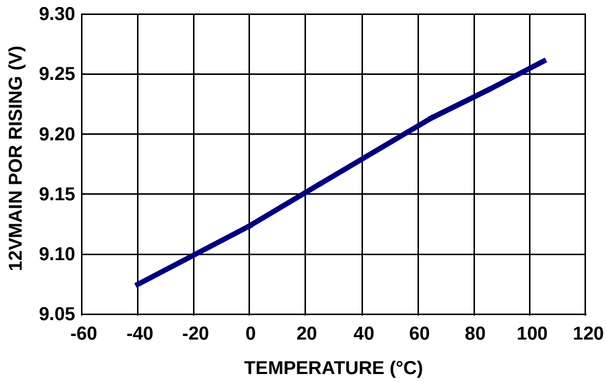


FIGURE 27. 12VMAIN RISING POR THRESHOLD VOLTAGE vs TEMPERATURE

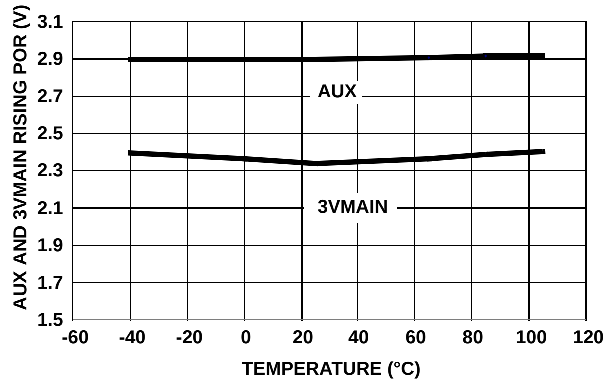


FIGURE 28. AUX AND 3VMAIN RISING POR THRESHOLD VOLTAGE vs TEMPERATURE

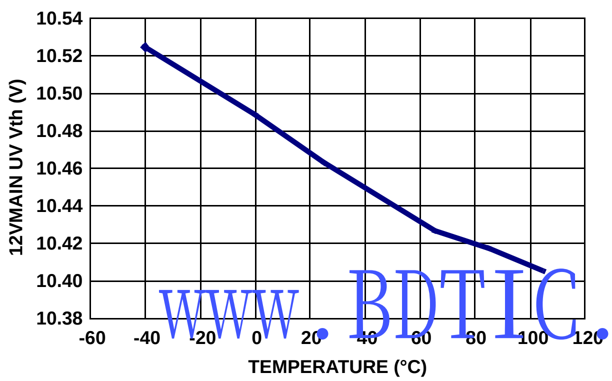


FIGURE 29. 12VMAIN POWER GOOD THRESHOLD VOLTAGE vs TEMPERATURE

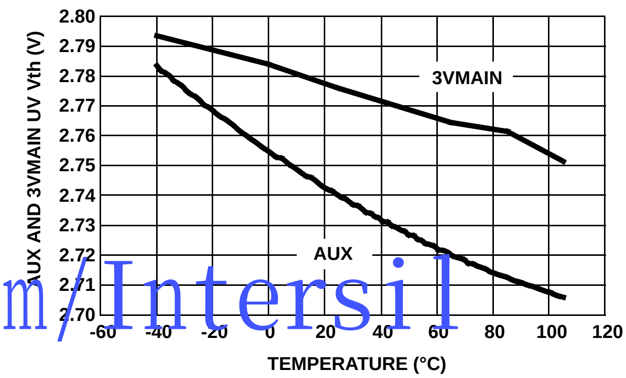


FIGURE 30. AUX AND 3VMAIN POWER GOOD THRESHOLD VOLTAGE vs TEMPERATURE

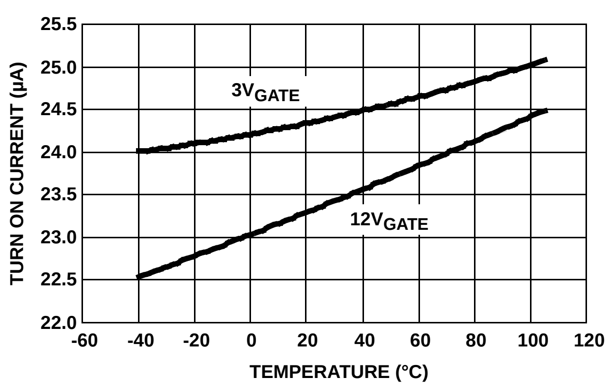


FIGURE 31. ISL6113 GATE TURN-ON CURRENT (ABS) vs TEMPERATURE

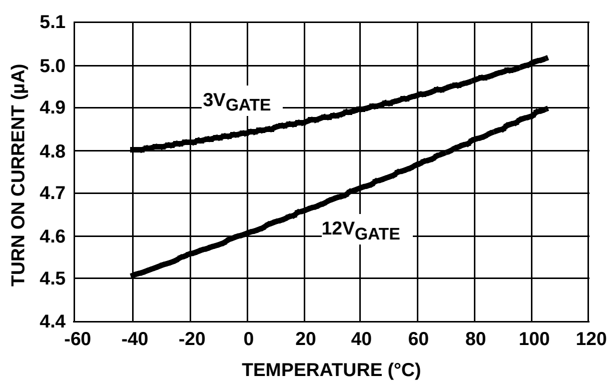


FIGURE 32. ISL6114 GATE TURN-ON CURRENT (ABS) vs TEMPERATURE

Typical Performance Curves (Continued)

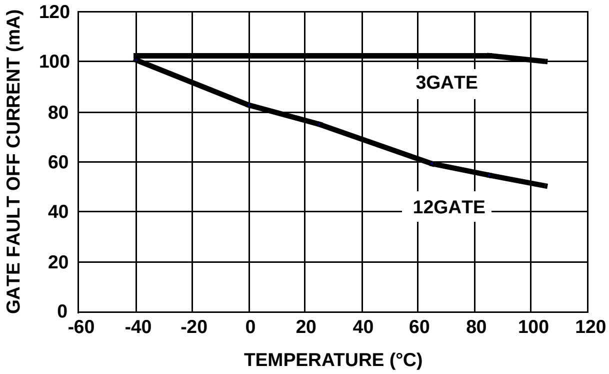


FIGURE 33. GATE FAULT OFF CURRENT (ABS) vs TEMPERATURE

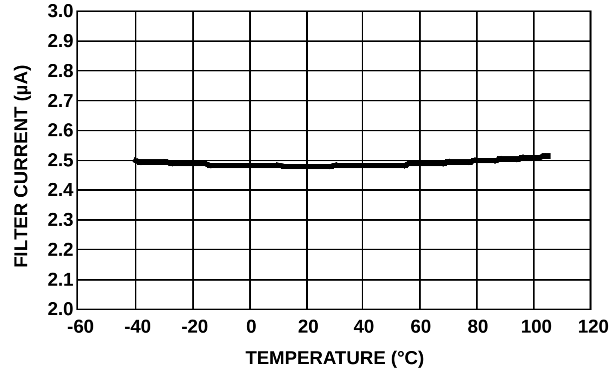


FIGURE 34. FILTER CHARGE CURRENT vs TEMPERATURE

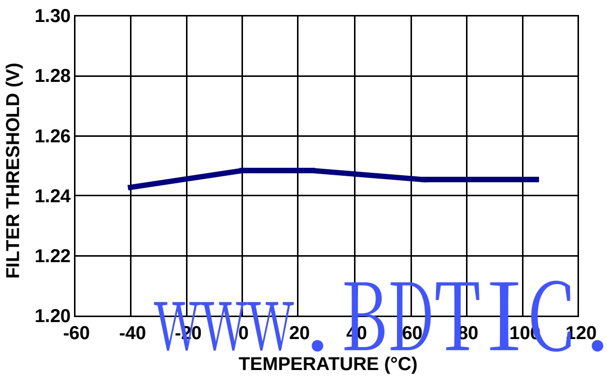


FIGURE 35. FILTER THRESHOLD VOLTAGE vs TEMPERATURE

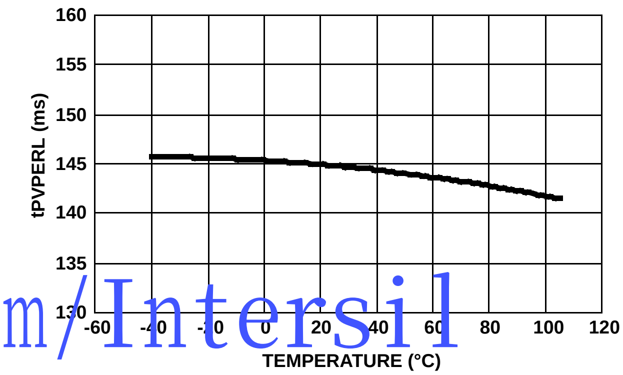


FIGURE 36. t_{PVPERL} vs TEMPERATURE

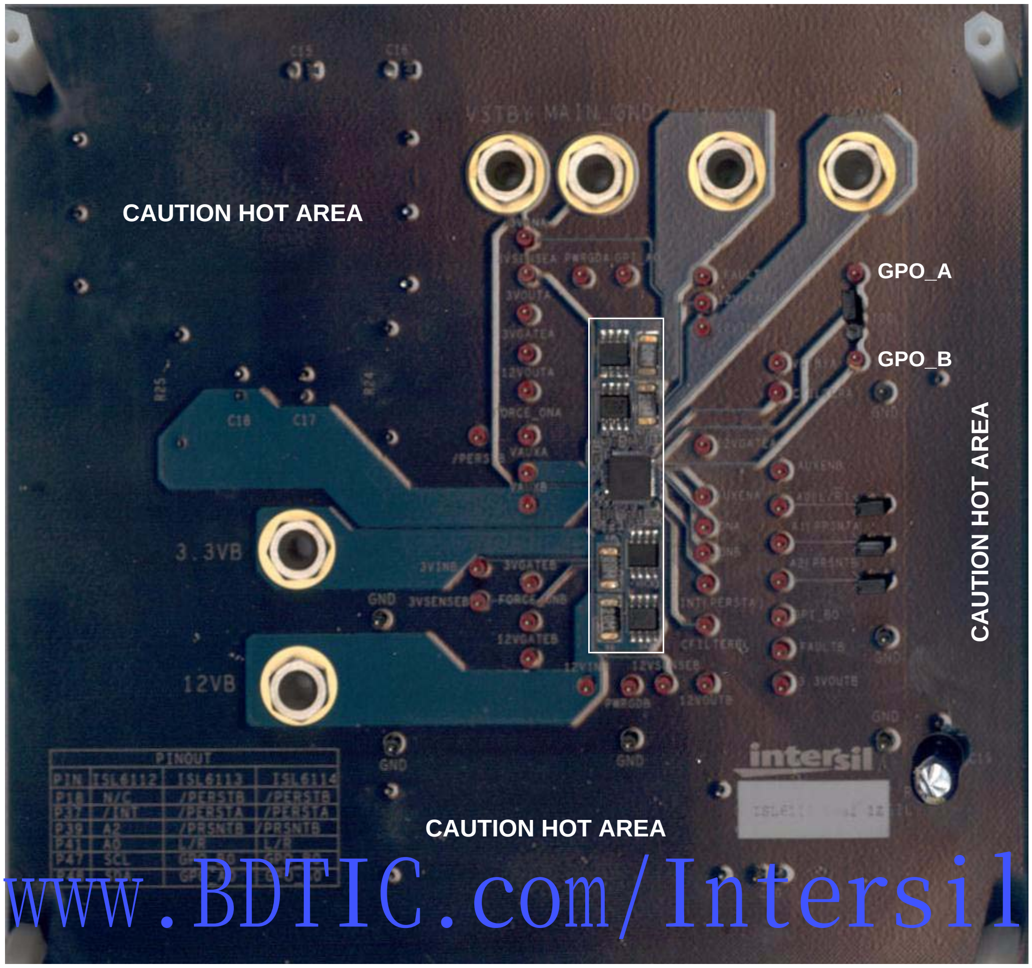


FIGURE 37. ISL6113EVAL1Z, ISL6114EVAL1Z BOARD PHOTOGRAPH

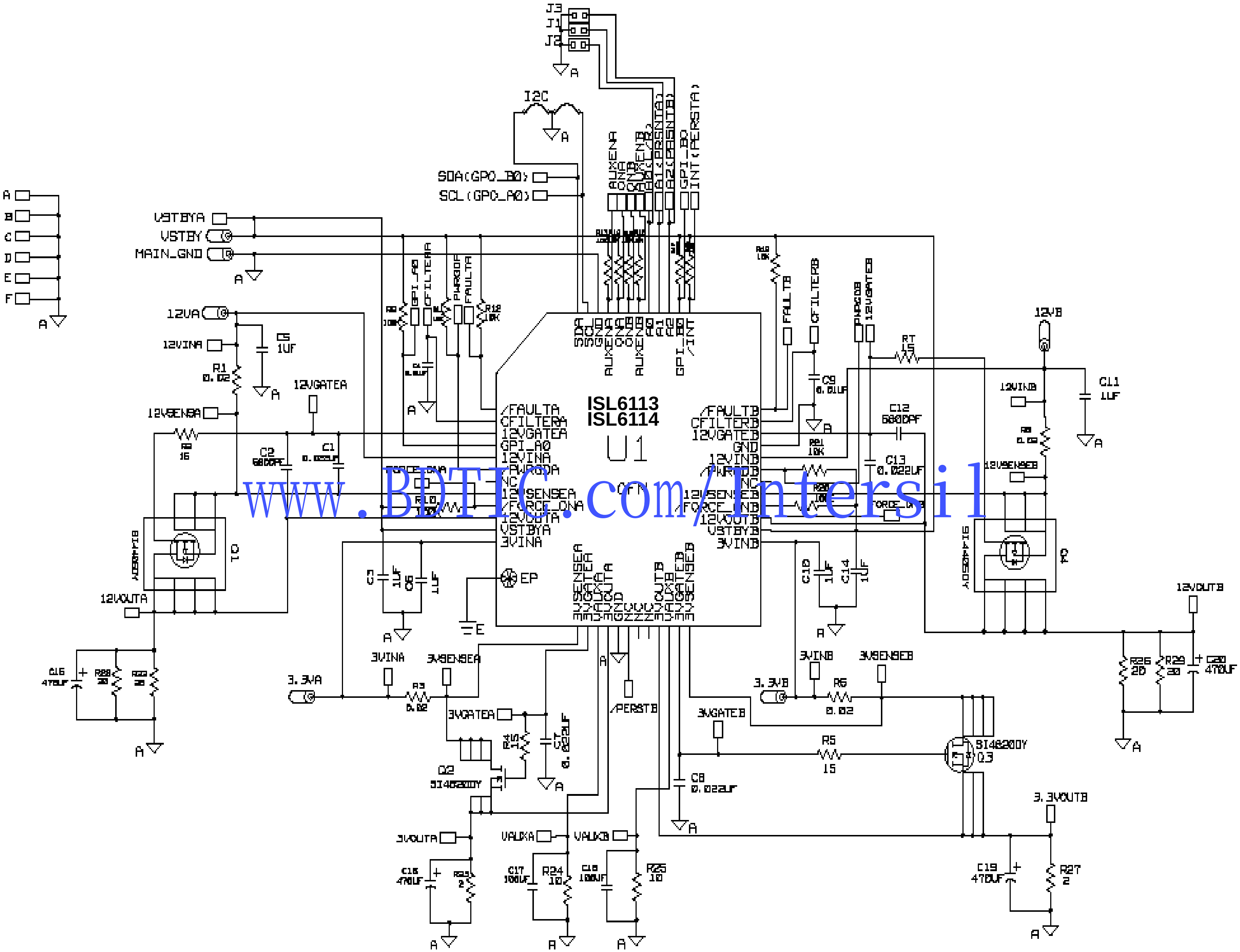


FIGURE 38. ISL6113EVAL1Z, ISL6114EVAL1Z BOARD SCHEMATIC

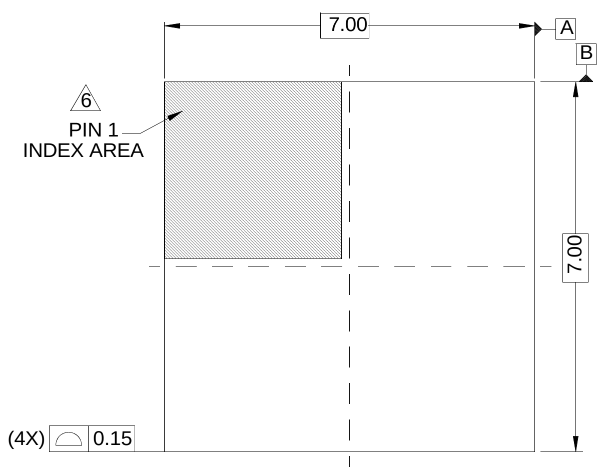
TABLE 5. ISL6113EVAL1Z, ISL6114EVAL1Z COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	**ISL6113 or ISL6114**	PCI-Express Dual Slot Hot Plug Controller
Q1, Q4	Voltage Rail Switches	SI4405DY or equivalent, P-Channel MOSFET
Q2, Q3	Voltage Rail Switches	SI4820DY or equivalent, N-Channel MOSFET
R1, R3, R6, R8	Current Sense Resistor	0.020Ω 1%, 2512
R9, R10, R17, R20	Pull-up resistors on $\overline{\text{FORCE_ON}}$ and GPI Inputs	100kΩ, 0201
R11, R12, R13, 14, R15, R16, R18, 19, R21	I/O Pull-up resistors	10kΩ, 0201
R2, R4, R5, R7	FET gate series resistance	15Ω, 0201
C1, C7, C8, C13	ISL6113EVAL1Z 3VMAIN FET gate capacitance	22nF 10%, 16V, 0402
C1, C7, C8, C13	ISL6114EVAL1Z 3VMAIN FET gate capacitance	open
C3, C5, C6, C10, C11, C14	MAIN and VSTBY decoupling capacitance	1µF 10%, 6.3V, 0402
C2, C12	ISL6113 12VMAIN FET gate to drain capacitance	6.8nF 10%, 6.3V, 0201
C2, C12	ISL6114 12VMAIN FET gate to drain capacitance	open
C4, C9	C_{FILTER} capacitance (5ms)	0.01µF 10%, 6.3V, 0201
R24, R25	AUX Load Resistance	10Ω 20%, 3W
C17, C18	AUX Load Capacitance	100µF 20%, 25V, Radial Electrolytic
R22, R26, R28, 29	12VMAIN Load Resistance	20Ω 20%, 10W
R23, R27	3VMAIN Load Resistance	2Ω 20%, 10W
C15, C16, C19, C20	12VMAIN and 3VMAIN Load Capacitance	470µF 20%, 16V, Radial Electrolytic

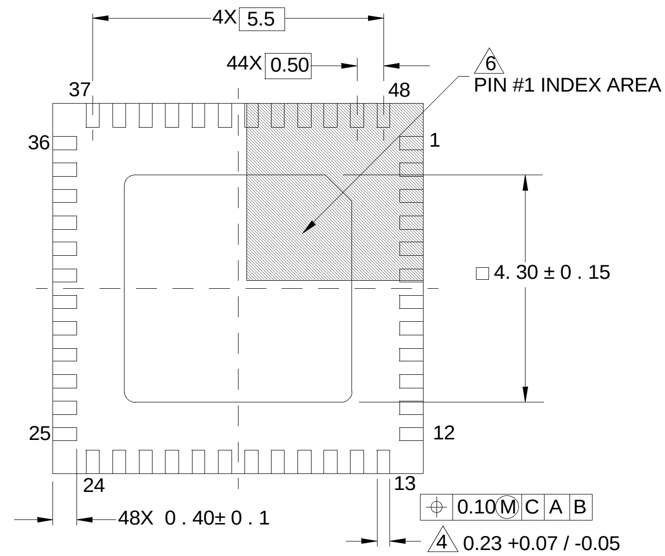
Package Outline Drawing

L48.7x7

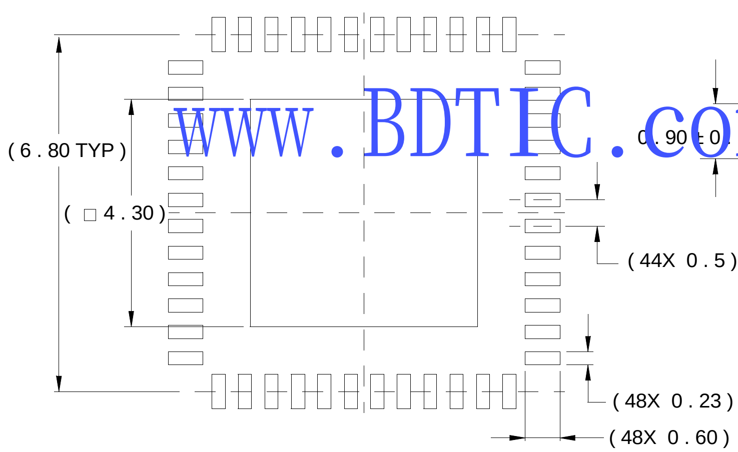
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



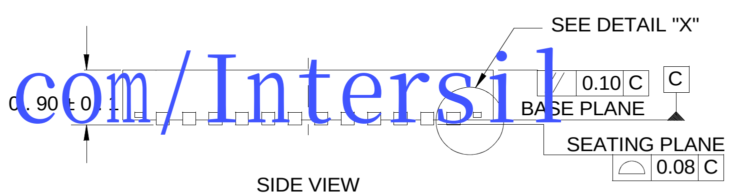
TOP VIEW



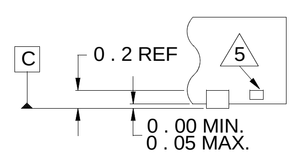
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.